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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MAHMOUDI, HASSAN	

ART UNIT	PAPER NUMBER
2175	13

DATE MAILED: 06/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PPG

Office Action Summary	Application 09/499,598	Applicant(s) HENNIGER ET AL.	
	Examiner Tony Mahmoudi	Art Unit 2175	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

SAM RIMELL
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's Request for Continued Examination (RCE) submission filed on 19-April-2004 has been entered. In addition, the Preliminary Amendment filed on 19-April-2004 has been entered for the continued examination of this application.

Remarks

2. In response to communications filed on 19-April-2004, claims 1-18 are cancelled, and new claims 19-32 are added, per applicant's request. Therefore, claims 19-32 are presently pending in the application.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claim 19 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Rasmussen et al (U.S. Patent No. 6,449,732.)

As to claim 19, Rasmussen et al teaches an apparatus (see Abstract, and see column 36, lines 59-60) comprising:

a first printed circuit board (see column 4, lines 15-21, and see column 5, line 16);

a processor mounted to the first printed circuit board (see column 5, lines 13-17), wherein the processor comprises a development port (see column 4, lines 59-66);

a system bus (see column 2, lines 21-22) formed on the first printed circuit board and coupled to the processor (see column 2, lines 61-67);

a second bus (see figure 2) formed on the first printed circuit board and coupled to the development port (see column 4, line 53 through column 5, line 6.)

As to claim 25, Rasmussen et al as modified, teaches wherein the second bus comprises a serial data bus (see column 15, lines 34-45.)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that said subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 20 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rasmussen et al (U.S. Patent No. 6,449,732), in view of Anderson (U.S. Patent No. 6,003,130.)

As to claim 20, Rasmussen et al teaches the apparatus further comprising

a second printed circuit board (see figure 69, see column 4, lines 15-21, and see column 17, lines 31-38);

a first data storage device mounted on the second printed circuit board (see figure 4, and see column 30, lines 23-35),

a coupler, coupling the first printed circuit board to the second printed circuit board (see figure 16, and see column 17, lines 31-38), defining at least a first data communication path from the second printed circuit board to the first printed circuit board (see column 17, lines 39-62);

wherein the data can be transmitted from the first storage device, over the first communication path, the second bus, to the development port of the processor (see column 4, line 53 through column 5, line 6, see column 11, lines 28-38, and see column 13, lines 12-25.)

Rasmussen et al does not teach:

wherein the first data storage device stores boot-up code; and

wherein the boot-up code can be transmitted from the first storage device.

Anderson teaches an apparatus for selecting, detecting, and programming system bios in a computer system (see Abstract), in which he teaches:

wherein the first data storage device stores boot-up code (see Abstract, see figures 2 and 3, and see column 4, lines 33-43); and

wherein the boot-up code can be transmitted from the first storage device (see column 3, lines 13-17, and see column 8, lines 6-10.)

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Rasmussen et al to include wherein the first data storage device stores boot-up code; and wherein the boot-up code can be transmitted from the first storage device.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Rasmussen et al by the teachings of Anderson, because including wherein the first data storage device stores boot-up code; and wherein the boot-up code can be transmitted from the first storage device, would enable the system to transfer boot-up code between different memory devices, as taught by Anderson (see column 3, lines 13-22.)

As to claim 31, Rasmussen et al teaches apparatus (see Abstract, and see column 36, lines 59-60) comprising:

a first printed circuit board (see column 4, lines 15-21, and see column 5, line 16) coupled (see figure 16) to a second printed circuit board (see figure 69, see column 4, lines 15-21, and see column 17, lines 31-38);

a processor mounted to the first printed circuit board (see column 5, lines 13-17), wherein the processor comprises a development port (see column 4, lines 59-66);

a system bus coupled to the processor (see column 2, lines 21-22, and lines 61-67);

a second bus coupled to the development port (see figure 2), wherein the second bus is formed on the first printed circuit board (see column 4, line 53 through column 5, line 6);

For the teachings of: "means for downloading a boot-up code from the second printed circuit board to the development port via the second bus, in response to a power on or reset of the apparatus", the applicant is kindly directed to the remarks and discussions made in claim 20 above, in view of Anderson's teachings.

7. Claims 21-24, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rasmussen et al (U.S. Patent No. 6,449,732), in view of Anderson (U.S. Patent No. 6,003,130), as applied to claims 20 and 31 above, and further in view of Tehranian et al (U.S. Patent No. 5,878,248.)

As to claims 21 and 32, Rasmussen et al as modified teaches a development port (see Rasmussen et al, see column 4, lines 59-66.)

Rasmussen et al as modified, still does not teach wherein the development port receives data from an emulator device external to the processor when the development port is coupled to the emulator device.

Tehranian et al teaches a device access controller (see Abstract), in which he teaches wherein the development port receives data from an emulator device external to the processor when the development port is coupled to the emulator device (see column 9, line 28 through column 10, line 27, and see column 13, line 22 through column 14, line 53.)

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Rasmussen et al, as modified, to include wherein the development port receives data from an emulator device external to the processor when the development port is coupled to the emulator device.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Rasmussen et al, as modified, by the teaching of Tehranian et al, because the development port receiving data from an emulator device external to the processor when the development port is coupled to the emulator device, would enable the system to optionally receive input from a virtual external storage emulator, when one is connected to the system, as taught by Tehranian et al (see column 13, lines 27-30.)

As to claim 22, Rasmussen et al as modified teaches wherein the second printed circuit board is configured to download the boot-up code to the development port automatically, in response to a power up or a reset of the apparatus (see Rasmussen et al, column 4, lines 59-66, and see Anderson, column 4, lines 44-67, and see column 6, lines 14-26.)

As to claim 23, Rasmussen et al as modified teaches wherein the first printed circuit board comprises a DRAM coupled to a memory controller (see Anderson, figure 2) and wherein the boot-up code comprises configuration information fir configuring the memory controller (see Anderson, column 2, line 59 through column 3, line 22, and see column 5, lines 50-67.)

As to claim 24, Rasmussen et al as modified teaches wherein the DRAM is coupled to the system bus (see Rasmussen et al, figure 2, and see column 7, lines 63-67, and see Anderson, figure 2.)

8. Claims 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (U.S. Patent No. 6,003,130), in view of Rasmussen et al (U.S. Patent No. 6,449,732.)

As to claim 26, Anderson teaches a method of booting up a system (see Abstract, and see column 5, lines 13-17), wherein the system comprises a motherboard coupled to daughterboard (see figure 2), wherein the daughterboard comprises a microprocessor, a system bus, and a second bus (see figure 2), wherein the microprocessor is coupled to the system bus and the second bus (see figure 2), the method comprising:

transmitting a first boot-up code from the motherboard via the second bus, in response to a power-on or reset of the system (see column 3, lines 13-17, see column 4, lines 44-67, see column 6, lines 14-26, and see column 8, lines 6-10); and

using the boot-up code, in the microprocessor to perform a first boot-up operation (see column 5, lines 4-17.)

Anderson does not teach:

wherein the microprocessor comprises a development port.

Rasmussen et al teaches a method and apparatus for processing control (see Abstract), in which he teaches wherein the microprocessor comprises a development port (see column 4, line 53 through column 4, line 6.)

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Anderson to include wherein the microprocessor comprises a development port.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Anderson by the teaching of Rasmussen et al, because including wherein the microprocessor comprises a development port, would enable the system to be used for interface with a development computer system or as a slave interface, where each processor module also contains one optional port for System Executive development or LAN support, as taught by Rasmussen et al (see column 4, lines 59-63.)

As to claim 27, Anderson as modified, teaches wherein the boot-up operation comprises configuring a port of the microprocessor that is different from the development port (see Rasmussen et al, column 16, lines 33-50, and see column 24, lines 19-20.)

As to claim 28, Anderson as modified teaches wherein the daughterboard comprises a DRAM and a memory controller (see Anderson, figure 2, where "memory controller" is read on "system controller **14**"), and wherein the boot-up operation comprises configuring the memory controller (see Anderson, column 3, lines 23-36.)

As to claim 29, Anderson as modified teaches wherein the daughterboard comprises a DRAM coupled to the system bus (see Anderson, figure 2), and wherein the method further comprises transmitting data from the mother board to the DRAM via the system bus (see Anderson, column 3, lines 13-17, and see column 8, lines 6-10.)

As to claim 30, Anderson as modified teaches wherein the data comprises an operating system for the microprocessor (see Anderson, figure 2, and see column 1, lines 56-67.)

Conclusion

9. Any inquiries concerning this communication or earlier communications from the examiner should be directed to Tony Mahmoudi whose telephone number is (703) 305-4887. The examiner can normally be reached on Mondays-Fridays from 08:00 am to 04:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici, can be reached at (703) 305-3830.

tm

May 27, 2004

SAM RIMELL
PRIMARY EXAMINER